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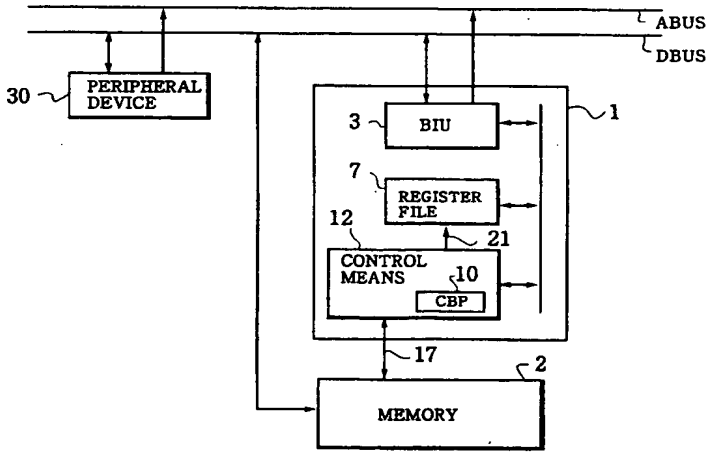
(54) Microprocessor and data processing system with register file.

(57) A microprocessor having a register file (7) inside is so combined with an external memory (2) through a dedicated high-speed bus that the memory operates as a bank for said register file. This microprocessor further has means (12) for controlling a data transfer with said memory (2) or peripheral devices (30). When an address information to access said memory (2) is input to this microprocessor in order to control a data transfer between said memory (2) and a peripheral device (30), said control means (12) finds if the accessed area in said memory (2) is now in use as a bank for said register file (7), or not. When it is in use, said control means (12) controls a data transfer between said peripheral device (30) and said register file (7), instead of controlling the data transfer between said memory (2) and said peripheral device (30). So, said peripheral device can always access the newest information in said memory.

FIG.1



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which the bank now in use in register file 7 is stored.

The third feature of the present invention is in the fact that said control means 12 has an adder-subtracter 25 (or an adder, shown in Fig. 2) in addition to said pointer 10, so as to compare the address information input, from peripheral device 30 or microprocessor 1, with the content in said pointer 10.

The fourth feature of the present invention provides a data processing system, which is comprised of the following as shown in Fig. 1: a microprocessor 1 which has the structure having said first, second, or third feature; memory 2 which is mapped on the address map of this data processing system; at least one peripheral device 30; data bus DBUS which connects among microprocessor 1, peripheral device 30, and memory 2; address bus ABUS which connects between microprocessor 1 and peripheral device 30; and dedicated bus 17 which connects microprocessor 1 with memory 2.

According to the first feature of the present invention, control means 12 has a function to find if peripheral device 30 or microprocessor 1 itself has accessed said address area, which corresponds to the bank now in use, in said memory 2 or not. When control means 12 finds that the accessed area in memory 2 corresponds to the address area in which the bank now in use is stored, it controls a data transfer between register file 7 and peripheral device 30 or microprocessor 1, instead of controlling a data transfer between memory 2 and peripheral device 30 or microprocessor 1. This is because the newest information concerning about the accessed area in memory 2 is now in said register file. On the other hand, when control means 12 finds that the accessed area in memory 2 does not correspond to said address area in which the bank now in use in register file 7 is stored, it controls a data transfer between memory 2 and peripheral device 30 or microprocessor 1 itself. As a result, peripheral device 30 or the microprocessor 1 can always obtain the newest information concerning about the accessed area in memory 2, even in the case where the area is used as the bank now in use in register file 7.

According to the second feature of the present invention, pointer 10 holds the first address of an memory area in which the bank now in use in register file is stored. Therefore, by comparing the address information, accessed by peripheral device 30 or microprocessor 1, with the content in said pointer 10, control means 12 can easily find if said address information corresponds to said address area, in which the bank now in use in register file is stored, or not. When it corresponds to said address area, means 12 controls a data transfer between register file 7 and peripheral device 30 or microprocessor 1, instead of controlling a data transfer between memory 2 and peripheral device 30 or microprocessor 1.

According to the third feature of the present invention, a subtraction is carried out between the content in said pointer 10 and a part of said address information. As a result, control means 12 can easily find if said address information corresponds to said address area in which the bank now in use in register file 7 is stored.

According to the fourth feature of the present invention, memory 2 is combined with register file 7 contained in microprocessor 1, so as to operate register file 7 as a bank. In this case, the data transfer between register file 7 and memory 2 is controlled through dedicated bus 17, so that the data transfer can be controlled at a high speed. In addition, in the case where peripheral device 30 or microprocessor 1 itself accesses memory 2, microprocessor 1 has a function to find if they have accessed a particular area in said memory 2, the area which is now in use as a bank in said register 7. Therefore, if the address information accessed by peripheral device 30 or microprocessor 1 corresponds to said area now in use as a bank, microprocessor 1 controls the data transfer between said register file 7 and peripheral device 30 or microprocessor 1, instead of controlling the data transfer between memory 2 and peripheral device 30 or microprocessor 1. So, peripheral device 30 or microprocessor 1 can always access the newest information in memory 2, even in the case where the accessed area is now in use as a bank in register file 7.

These and other objectives, features, and advantages of the present invention will be more apparent from the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the principle of the present invention; and

Fig. 2 shows the structure of a microprocessor and a data processing system according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Fig. 2 shows the structure of a microprocessor according to one embodiment of the present invention, and a data processing system in which said microprocessor is incorporated.

As shown in the figure, the data processing system is comprised of a microprocessor (referred to as MPU, below) 1, bank RAM 2, an external

operating speed of MPU 1. To that end, dedicated high speed bus 17, which has a larger bus width than that of external data bus DBUS, is used in order to transfer data at a high speed between bank RAM 2 and register file 7.

Exchange of banks is controlled in order to store a bank, now in use by MPU 1, into bank RAM 2 due to the generation of interruption. Such exchange is also controlled in order to transfer a bank, to be used in an interrupt routine, from bank RAM 2 to register file 7. In actuality, when an interruption occurs, bank control unit 9 generates address information 21 for register file 7 and bank RAM address control signal 18 for bank RAM 2 in every data transfer unit one after another, so as to store banks into bank RAM 2. In this case, address information 21 and bank RAM address control signal 18 are produced in adder-subtracter 25 contained in bank control unit 9, by executing arithmetic operations on the content in current bank pointer 10. As mentioned before, current bank pointer 10 holds the data (or the address itself) indicating the address area of a bank in bank RAM 2, the bank which is now in use by MPU 1.

In said case, if the interruption takes place under the control by external signals, the contents in a program status word PSW, a stack pointer PC, and previous bank pointer 11 should also be stored into bank RAM 2. As mentioned before, previous bank pointer 11 holds the data (or the address itself) indicating the return area of another bank in bank RAM 2, the bank which is to be recalled by register file 7 at the completion of the task under operation. On the other hand, in the case of interruption by program, the contents in program counter (PC), program status word (PSW), and previous pointer 11 should be stored into a stack memory.

Next, the content in current bank pointer 10 is copied into previous bank pointer 11. Thereafter, according to the generation of an interruption, new bank information based on the interrupt vectors is processed to produce a new address data of bank RAM 2, the data which correspond to a new bank to be newly used in the interrupt routine. In this address of bank RAM 2, a new bank, which will be available in MPU to execute the interrupt routine, is stored. The new address information thus obtained is then transferred into current bank pointer 10.

The new content in current bank pointer 10 obtained as mentioned above is processed in adder-subtracter 25 in bank control unit 9. Thus, bank control unit 9 again produces address information 21 for register file 7 and bank RAM address control signal 18 for bank RAM 2 in every data transfer unit one after another, so as to transfer a required bank from bank RAM 2 to register file 7. In this case, if the interruption occurs according to the control by a program, the content in previous pointer 11 is changed to be specially fixed data. According to these data, it is recognized that program pointer PC, program status word PSW, and previous bank pointer 11, which are required to return from the interruption, are stored not in bank RAM 2 but in the stack memory.

The bank exchange by program is controlled when a programmer manages banks with intention using a subroutine. In this case, only the content in current bank pointer 10 should be changed. Therefore, in the same manner as that of the interruption process mentioned above, bank control unit 9 controls arithmetic operations to the content in current bank pointer 10 using adder-subtracter 25, according to control signals from micro ROM 5. Thus, address information 21 for register file 7 and bank RAM address control signal 18 for bank RAM 2 are produced in unit 9 every data transfer unit one after another, so as to transfer a required bank from bank RAM 2 to register file 7.

The bank exchange for the return from the interruption is controlled according to a return instruction. Control signal 22 from micro ROM 5 is generated according to said return instruction. In this case, bank control unit 9 transfers the data in previous bank pointer 11 into current bank pointer 10. Thereafter, unit 9 controls arithmetic operations on the new content in current bank pointer 10 using adder-subtracter 25, and then, produces new address information 21 for register file 7 and bank RAM address control signal 18 for bank RAM 2 in every data transfer unit one after another. Thus, the bank to be recalled is transferred from bank RAM 2 to register file 7. In this case, if the interruption was made by external signals, program counter PC, program status word PSW, and previous bank pointer 11, each of which have been stored in bank RAM 2 at the generation of the interruption, are transferred into register file 7. On the other hand, in order to store the bank, which has been used in register file 7, the content in the bank should be transferred from register file 7 to bank RAM 2 using the bank exchange process by program. In the case of interruption by program, program counter PC, program status word PSW, and previous bank pointer 11 are recalled from the stack memory.

(2) In the case of a data transfer between bank RAM 2 and peripheral device 30

The data transfer between bank RAM 2 and peripheral unit 30 is an indispensable function for bank RAM 2 to operate in the same manner

bank, bank control unit 9 outputs the lower 11 bits of external address bus ABUS to bank RAM 2 without a change. Also, bank control unit 9 processes the bus start signal, read-write signal, and chip select signal contained in external control bus CBUS, and then, outputs the resulting signal as bank RAM address control signal 18. Thus, the content in bank RAM 2 is transferred into peripheral unit 30 through external data bus DBUS.

On the contrary, when the content in bank RAM 2 accessed by the peripheral device is in accord with the content in register file 7 which is now in use by MPU 1, bank control unit 9 outputs register file address control signal 21 to register file 7. This signal 21 is produced from external control bus CBUS and a 5 bit address signal, in which the higher 2 bits of the operation result in adder-subtracter 25 are placed in its higher part, and the lower 3 bits of external address bus ABUS are placed in its lower part. On the other hand, bank interface unit 8 connects the data bus from register file 7 with dedicated high-speed bus 17.

In said occasion, bank control unit 9 also controls bank RAM 2 using bank RAM address control signal 18, so that dedicated high speed bus 17 is connected with external data bus DBUS. However, the bus width of dedicated high-speed bus 17 deferes from that of external data bus DBUS. Accordingly, in order to connect high-speed bus 17 with data bus DBUS, the essential 16 bits data are taken out from dedicated high-speed bus 17 using the higher 2 bits among the lower 3 bits of external address bus ABUS. Then, said 16 bit data are made to run on external data bus DBUS. In this case, the content in bank RAM 2 is not accessed at all.

As explained above, when the content in bank RAM 2 accessed by a peripheral device is in accord with the content in register file 7, which is now in use as a bank by MPU 1, the data transfer is controlled between the peripheral device and register file 7 instead of bank RAM 2. In this case, the data in register file 7 run on external data bus DBUS in the same timing as that of the access for bank RAM 2.

In addition, when the content in bank RAM 2 accessed by the peripheral device is in accord with the content in register file 7, which is now in use as a bank by MPU 1, register file 7 is accessed instead of bank RAM 2. In this case, bank wait signal 23 notifies MPU 1 that register file 7 is now being accessed. Thus, the operation of MPU 1 is not influenced by said operation of the peripheral device.

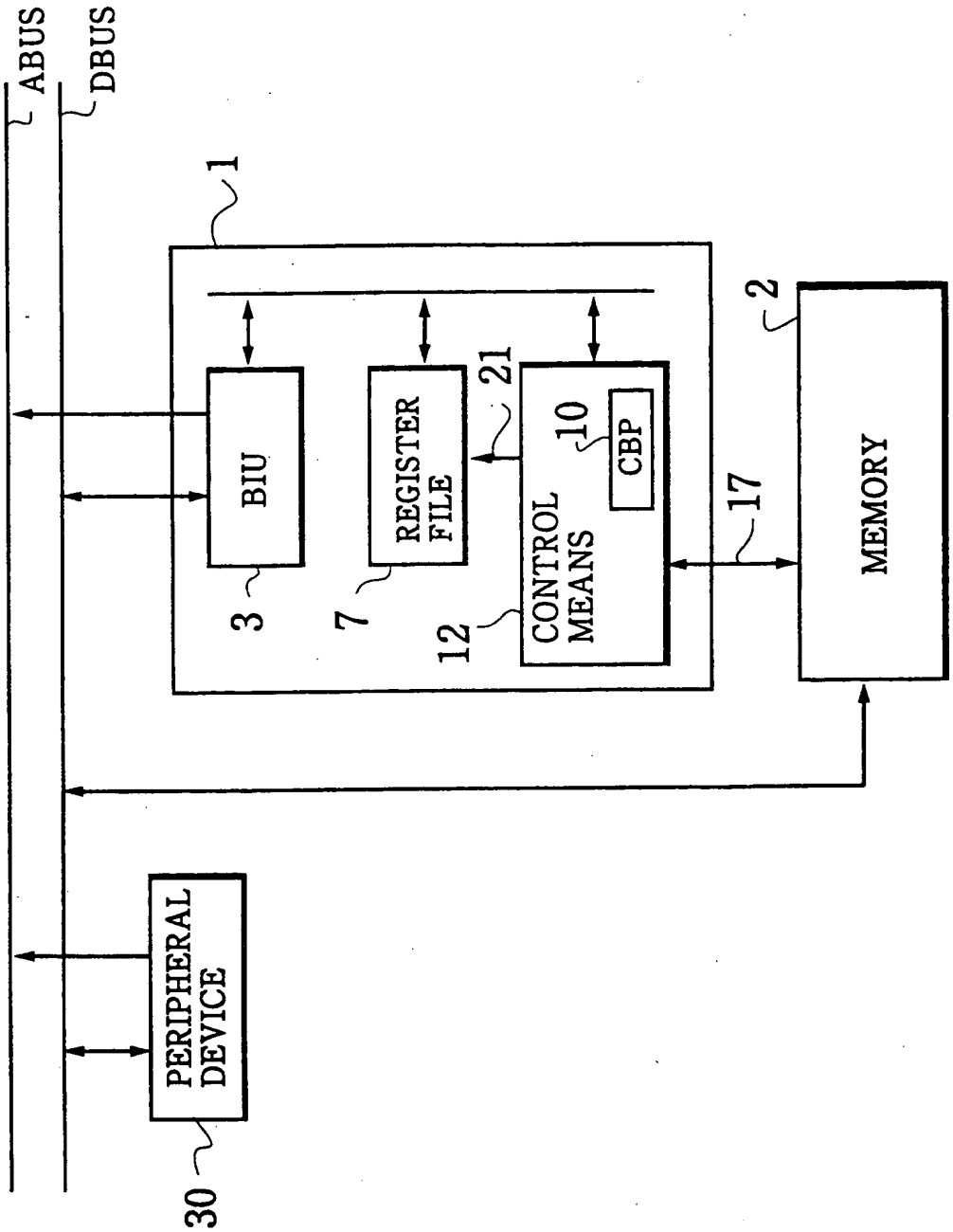
As explained above, the data processing system of this embodiment stores, into current bank pointer 10, of information concerning about the first address of an address area in bank RAM 2, the area which corresponds to the bank now in use in register file 7. The content in current bank pointer 10 is, then, compared with the address information which is input from peripheral device 30, so as to find if peripheral device 30 accesses a particular area in bank RAM 2, the area which corresponds to the bank now in use in register file 7, or not. As a result of said comparison, if the area in bank RAM 2 accessed by peripheral device 30 is found to correspond to the address area of the bank now in use in register file 7, data access is executed for register file 7 instead of bank RAM 2. Thus, peripheral device can always access the newest information in bank RAM 2.

In summary, the control means contained in the microprocessor of this invention has a function to find if a peripheral device or the microprocessor itself accesses a particular area in an external memory, the area which corresponds to the bank now in use by this microprocessor itself, or not. In the case where said area in the external memory is accessed, the control means controls a data transfer between a register file (bank) and said peripheral device or the microprocessor itself, instead of a data transfer between said external memory (bank RAM) and said peripheral device or the microprocessor itself. As a result, the microprocessor itself or said peripheral device can access the newest information in said external memory, even in the case where said area, corresponding to the bank now in use by this microprocessor, is accessed by them. In addition, said data transfer between the register file and the peripheral device or the microprocessor can be carried out through a dedicated high speed bus. So, this invention can provide a microprocessor and a data processing system, in which the newest information in an external memory can be correctly and efficiently accessed by a peripheral device or the microprocessor itself.

Claims

1. A microprocessor, comprising:
   a register file; and
   means for controlling the data transfer between said register file and an external memory which is connected to the present microprocessor itself through a dedicated bus;
   wherein said control means has a function to control a data transfer between said register file and a peripheral device, which is connected to said external memory through an external data bus, or the microprocessor itself, instead of a data transfer between said external memory and peripheral device or the microprocessor, when a particular address area in said external memory, the area which

FIG.1


ABUS
DBUS
1
BIU
3
REGISTER FILE
7
21
CONTROL MEANS
12
10
CBP
17
2
MEMORY
PERIPHERAL DEVICE
30

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EUROPEAN SEARCH REPORT

Application Number

EP 93 10 4091

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	MICROPROCESSORS AND MICROSYSTEMS, vol. 13, no. 9, November 1989, LONDON, GB; I.HAY ET AL 'TRON-Compatible 16/32-Bit Microprocessor' * abstract; figures 1-4,7,8,12-14 * * page 608, left column, line 41 - page 609, right column, line 35 * * page 610, right column, line 27 - page 611, left column, line 61 * * page 618, left column, line 20 - line 43 * * tables 1-3 *	1-7, 10-12	G06F9/46
Y	---	8,9	
Y	US-A-4 352 157 (NAMIMOTO ET AL) * abstract; figures 1,2,6-8 * * column 2, line 14 - line 55 * * column 3, line 33 - line 46 * * column 4, line 15 - line 54 * * column 5, line 67 - column 7, line 12 * * column 7, line 51 - column 10, line 59 *	8,9	
A	---	1,7,8,10	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	US-A-4 905 200 (PIDSOSNY ET AL) * the whole document *	1,3,5-8	G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 JUNE 1993	POWELL D.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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